WHAT IS CLAIMED IS:

1. An apparatus for re-synchronizing an input data signal to be transmitted as a serial signal having a data frame and idle pattern, in which the data frame has a certain length or less and has its start and end positions to be detected, and the idle pattern is transmitted in intervals other than the data frame and has a length of integer times as much as that of a known bit string, comprising:

a clock oscillator configured to generate a reference clock signal;

a first phase-locked loop oscillator configured to generate an input clock signal synchronized with the input data signal;

a second phase-locked loop oscillator configured to generate an output clock signal synchronized with the reference clock signal, a frequency of said output clock signal being approximately equal to that of said input clock signal, and a phase of said output clock signal being different from that of said input clock signal;

a serial-parallel converter configured to convert the input data signal into a first parallel data signals of a predetermined number of parallel bits and a second parallel data signals of a predetermined number of idle pattern bits in synchronization with the input clock signal;

a detector configured to detect the data frame and its start and end positions from the second parallel data signals as a data detection signal and a first take-in signal;

a data extension circuit configured to time-axially extend the first parallel data signals by a predetermined clock length in synchronization with the input clock signal in accordance with the first take-in signal, thereby outputting extended data signals of said predetermined number

of parallel bits;

a first signal generator configured to generate a second input take-in signal based on the data detection signal;

a second signal generator configured to generate a data interval signal by re-synchronizing the data detection signal with the output clock signal;

a third signal generator configured to generate a re-take-in signal of said predetermined number of parallel bits based on the second input take-in signal;

a data re-synchronizer configured to re-synchronize the extended data signals with the output clock signal to generate re-data signals of said predetermined number of parallel bits;

an idle pattern generator configured to self-generate an idle pattern as an idle signal, judge whether the input data signal is of the idle pattern or the data frame based on the data interval signal, output the self-generated idle signal if the input data signal is of the idle pattern, and output a delay signal and a selection signal if the input data signal is of the data frame;

a parallel-serial converter configured to convert the re-data signals into a serial signal in accordance with the re-take-in signal;

a data delay circuit configured to delay the serial signal in accordance with the delay signal; and

a data selector configured to select the idle signal and the delayed signal as an output data signal in accordance with the selection signal.

2. The apparatus according to claim 1, wherein said predetermined number of parallel bits is determined by an absorption of phase difference between the input clock signal

and the output clock signal, an avoidance of meta-stability, jitter, and skew, and an absorption of frequency deviation between the input clock signal and the output clock signal.

3. The apparatus according to claim 1, wherein said predetermined clock length is not less than said number of parallel bits.

4. The apparatus according to claim 1, wherein said frequency of said output clock signal is equal to that of said input clock signal.

5. The apparatus according to claim 1, wherein said frequency of said output clock signal is higher than that of said input clock signal.

6. An apparatus for re-synchronizing an input data signal to be transmitted as a serial signal having a data frame and idle pattern, comprising:

a clock oscillator configured to generate a reference clock signal;

a phase-locked loop oscillator configured to generate an input clock signal synchronized with the input data signal and an output clock signal synchronized with the reference clock signal, a frequency of said output clock signal being approximately equal to that of said input clock signal, and a phase of said output clock signal being different from that of said input clock signal;

a serial-parallel converter configured to convert the input data signal into a first parallel data signals of a predetermined number of parallel bits and a second parallel data signals of a predetermined number of idle pattern bits in synchronization with the input clock signal;

an detector configured to detect the data frame and its start and end positions from the second parallel data signals as a data detection signal;

a data extension circuit configured to time-axially extend the first parallel data signals by a predetermined clock length in synchronization with the input clock signal based on the data detection signal, thereby outputting extended data signals of said predetermined number of parallel bits;

a data re-synchronizer configured to re-synchronize the extended data signals with the output clock signal to generate re-data signals of said predetermined number of parallel bits;

an idle pattern generator configured to self-generate an idle pattern as an idle signal, judge whether the input data signal is of the idle pattern or the data frame based on the data detection signal, output the self-generated idle signal if the input data signal is of the idle pattern, and output a delay signal and a selection signal if the input data signal is of the data frame;

a parallel-serial converter configured to convert the re-data signals into a serial signal in accordance with the re-take-in signal;

a data delay circuit configured to delay the serial signal based on the delay signal; and

a data selector configured to select the idle signal and the delayed signal as an output data signal based on the selection signal.

7. A method for re-synchronizing an input data signal to be transmitted as a serial signal having a data frame and idle pattern, in which the data frame has a certain length or less and has its start and end positions to be

detected, and the idle pattern is transmitted in intervals other than the data frame and has a length of integral times as much as that of a known bit string, comprising the steps of:

generating a reference clock signal;

generating an input clock signal synchronized with the input data signal;

generating an output clock signal synchronized with the reference clock signal, a frequency of said output clock signal being about equal to that of said input clock signal, a phase of said output clock signal being different from that of said input clock signal;

converting the input data signal into a first parallel data signals of a predetermined number of parallel bits and a second parallel data signals of a predetermined number of idle pattern bits in synchronization with the input clock signal;

detecting the data frame and its start and end positions from the second parallel data signals as a data detection signal and a first take-in signal;

time-axially extending the first parallel data signals by a predetermined clock length in synchronization with the input clock signal in accordance with the first take-in signal, thereby outputting extended data signals of said predetermined number of parallel bits;

generating a second input take-in signal based on the data detection signal;

generating a data interval signal by re-synchronizing the data detection signal with the output clock signal;

generating configured to generate a re-take-in signal of said predetermined number of parallel bits based on the second input take-in signal;

re-synchronizing the extended data signals with the output clock signal to generate re-data signals of said predetermined number of parallel bits;

self-generating an idle pattern as an idle signal, judging whether the input data signal is of the idle pattern or the data frame based on the data interval signal, outputting the self-generated idle signal if the input data signal is of the idle pattern, and outputting a delay signal and a selection signal if the input data signal is of the data frame;

converting the re-data signals into a serial signal in accordance with the re-take-in signal;

delaying the serial signal in accordance with the delay signal; and

selecting the idle signal and the delayed signal as an output data signal in accordance with the selection signal.

8. The method according to claim 7, wherein said predetermined number of parallel bits is determined by an absorption of phase difference between the input clock signal and the output clock signal, an avoidance of meta-stability, jitter, and skew, and an absorption of frequency deviation between the input clock signal and the output clock signal.

9. The method according to claim 7, wherein said predetermined clock length is not less than said number of parallel bits.

10. The method according to claim 7, wherein said frequency of said output clock signal is equal to that of said input clock signal.

11. The method according to claim 7, wherein said

frequency of said output clock signal is higher than that of said input clock signal.